



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/573,717	03/28/2006	Yoshitake Hayashi	10873.1876USWO	2188

53148 7590 05/05/2008
HAMRE, SCHUMANN, MUELLER & LARSON P.C.
P.O. BOX 2902-0902
MINNEAPOLIS, MN 55402

EXAMINER

CHEN, XIAOLIANG

ART UNIT	PAPER NUMBER
----------	--------------

2841

MAIL DATE	DELIVERY MODE
-----------	---------------

05/05/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/573,717	HAYASHI ET AL.	
	Examiner	Art Unit	
	XIAOLIANG CHEN	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 March 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6,9-13,15-20,22 and 23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6 and 9 is/are rejected.
- 7) ☒ Claim(s) 10-13,15-20,22 and 23 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Amendment

1. Acknowledgement is made of Amendment filed 03-14-08.
2. Claim 1 is amended.
3. Claim 24 is canceled.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

For one of the new added limitation; “so that a shape of the cavity is altered to coincide with outer dimensions of the mounted electronic component” is a new matter, and which is not supported by the original disclosure.

Applicant states in the Remarks, that claim 1 has been amended as supported by the specification at page 17, line 27—page 18, line 6 and Figures 1 and 3D.

The examiner reviewed the original disclosure and found no such support at all. There are no words related to “shape of the cavity is altered” to “coincide with outer dimensions” of the mounted electronic component at page 17, line 27—page 18, line 6. Also, the Figures 1 and 3D do not show these features.

Response to Arguments

6. Applicant's arguments filed 03-14-08 have been fully considered but they are not persuasive.

Applicant's arguments and responses:

A. Kanzawa does not disclose or suggest a first electrical insulating sheet with a cavity formed penetrating therethrough for mortaring an electronic component, and a second electrical insulating sheet formed by lamination over the first sheet to cover the cavity, as claim 1 requires.

This argument is not persuasive because

The examiner indicated in last Office Action that Kanzawa et al. does not disclose on the first electrical insulating sheet with a cavity formed penetrating therethrough. The cavity is taught by Kwong.

B. For the reference of Kwong, the argument has been considered but is moot the new amended limitation; “thereafter altering a shape of the cavity to fix the electronic component in the insulating sheet and simultaneously”.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanzawa et al. (US20040078969) in view of Kwong (US6732428).

Re claim 1, Kanzawa et al. show and disclose

A method for manufacturing a component built-in module, comprising the steps of:

one principal surface of a first electrical insulating sheet (101, fig. 1),

Kanzawa et al. does not disclose

on the first electrical insulating sheet with a cavity formed penetrating therethrough,

In the same field of an electronic device, Kwong teaches:

on the first electrical insulating sheet with a cavity formed penetrating therethrough (cavity 192, fig. 2),

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the first insulating layer of Kanzawa et al. by cutting a cavity as taught by Kwong, since Kwong states in [ABSTRACT], "The cavity is sized to accommodate an electronic component therein".

Kanzawa et al. further show and disclose

laminating a second electrical insulating sheet (103, fig. 1), so as to cover the cavity, so that a third electrical insulating sheet (101 and 103, fig. 1) comprising the first electrical insulating sheet and the second electrical insulating sheet is formed;

forming a via hole (115, fig 12) so as to penetrate through the third electrical insulating sheet; filling the via hole with a conductive resin paste (as via paste material, a mixture of an electroconductive powder and a resin is used [0074]);

disposing a first wiring board (101, fig. 11) with a first wiring pattern (102) and an electronic component (108) mounted on the first wiring pattern so as to face a principal surface of the third electrical insulating sheet at which the cavity has been formed, and disposing a second wiring board (101, fig. 9) with a second wiring pattern (102) so as to be opposed to the first wiring board with respect to the third electrical insulating sheet;

stacking the first wiring board, the third electrical insulating sheet and the second wiring board so that the electronic component is built in the cavity and the

via hole is disposed between the first wiring pattern and the second wiring pattern (fig. 13); and

applying heat and pressure (as shown in FIG. 22, the carrier 1 on which the circuit pattern 12 is formed and the electrical insulating layer 4 in which the vias 5 are formed are superposed one on another while being aligned in predetermined positions, followed by heating and pressing. The bare semiconductor element 8 and the circuit pattern 12 are thereby embedded in the electrical insulating layer 4. [0007]) by hot pressing to the stacked first wiring board, third electrical insulating sheet and second wiring board so that a shape of the cavity is altered to coincide with outer dimensions of the mounted electronic component {Examiner's Notes: When applying heat and pressure to the electronic component mounted in the cavity (modified by Kwong above) of the non-conductive film (Kanzawa), the non-conductive film would be soften (Under the heating and pressing the insulating layer may be maintained in a half-cured state to facilitate embedding [Kanzawa, paragraph 0075]) and the shape of the cavity would be altered and to coincide with outer dimensions of the mounted electronic component.}, so that the electronic component is fix in the cavity and the first wiring pattern and the second wiring pattern are connected electrically through a via conductor (5, fig. 22) made of the conductive resin paste.

Re claim 2, Kanzawa et al. show and disclose

The method for manufacturing a component built-in module according to claim 1,

Kanzawa et al. does not disclose

wherein the third electrical insulating sheet is formed by further laminating a fourth electrical insulating sheet with a cavity formed penetrating therethrough so as to be opposed to the first electrical insulating sheet with respect to the second electrical insulating sheet, the second wiring board disposed to be opposed to the first wiring board further comprises an electronic component mounted on the second wiring pattern, and the first wiring board, the third electrical insulating sheet and the second wiring board are stacked so that the electronic component mounted on the second wiring pattern is built in the cavity formed in the fourth electrical insulating sheet.

In the same field of an electronic device, Kwong teaches:

wherein the third electrical insulating sheet is formed by further laminating a fourth electrical insulating sheet (132, fig. 2) with a cavity (164, fig. 2) formed penetrating therethrough (fig. 2) so as to be opposed to the first electrical insulating sheet with respect to the second electrical insulating sheet, the second wiring board disposed to be opposed to the first wiring board further comprises an electronic component (156, fig. 2) mounted on the second wiring pattern, and the first wiring board, the third electrical insulating sheet and the second wiring board are stacked so that the electronic component mounted on the second wiring pattern is built in the cavity formed in the fourth electrical insulating sheet (fig. 2).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the electronic device of Kanzawa et al. by adapting a fourth electrical insulating sheet and an electronic component as taught by Kwong, since Kwong states in [ABSTRACT], "The cavity is sized to accommodate an electronic component therein".

Re claim 3, Kanzawa et al. show and disclose

The method for manufacturing a component built-in module according to claim 1,

Kanzawa et al. does not disclose

wherein the second electrical insulating sheet comprises a cavity penetrating therethrough, the cavity being formed at a position that does not overlap with a position of the cavity formed in the first electrical

insulating sheet, the second wiring board disposed to be opposed to the first wiring board further comprises an electronic component mounted on the second wiring pattern, and the first wiring board, the third electrical insulating sheet and the second wiring board are stacked so that the electronic component mounted on the second wiring pattern is built in the cavity formed in the second electrical insulating sheet.

In the same field of an electronic device, Kwong teaches:

wherein the second electrical insulating sheet comprises a cavity (176, fig. 2) penetrating therethrough, the cavity being formed at a position that does not overlap with a position of the cavity (192, fig. 2) formed in the first electrical insulating sheet, the second wiring board disposed to be opposed to the first wiring board further comprises an electronic component (170, fig. 2) mounted on the second wiring pattern, and the first wiring board, the third electrical insulating sheet and the second wiring board are stacked so that the electronic component mounted on the second wiring pattern is built in the cavity formed in the second electrical insulating sheet (fig. 2).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the second electrical insulating sheet of Kanzawa et al. by adapting a cavity and an electronic component as taught by Kwong, since Kwong states in

[ABSTRACT], "The cavity is sized to accommodate an electronic component therein".

Re claim 4, Kanzawa et al. show and disclose

The method for manufacturing a component built-in module according to claim 1,

wherein the first wiring board further comprises a supporting member (a supporting member 0014]) with the first wiring pattern formed thereon, and after applying heat and pressure by the hot pressing, the supporting member is removed (removing the pattern layer from the supporting member [0016]).

Re claim 5, Kanzawa et al. show and disclose

The method for manufacturing a component built-in module according to claim 1,

Kanzawa et al. does not disclose

wherein the cavity formed in the first electrical insulating sheet comprises a first cavity and a second cavity, the second electrical insulating sheet comprises a third cavity communicating with the second cavity, the electronic component mounted on the first wiring pattern of the first wiring board comprises a first electronic component and a second electronic component whose height is larger than that of the first electronic component, and the first wiring board, the third electrical insulating sheet and the second wiring board are stacked so that the first electronic

component is built in the first cavity and the second electronic component is built in the second cavity and the third cavity.

In the same field of an electronic device, Kwong teaches:

wherein the cavity formed in the first electrical insulating sheet comprises a first cavity (190, fig. 2) and a second cavity 176), the second electrical insulating sheet comprises a third cavity communicating with the second cavity (192), the electronic component mounted on the first wiring pattern of the first wiring board comprises a first electronic component (190) and a second electronic component (170) whose height is larger than that of the first electronic component (fig. 2), and the first wiring board, the third electrical insulating sheet and the second wiring board are stacked so that the first electronic component is built in the first cavity and the second electronic component is built in the second cavity and the third cavity (fig. 2).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the electrical insulating sheets of Kanzawa et al. by adding cavities and adding electronic components to fit in the cavities as taught by Kwong, since Kwong states in [ABSTRACT], "The cavity is sized to accommodate an electronic component therein".

Art Unit: 2859

9. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kanzawa et al. in view of Kwong as applied to claim 1 above, and further in view of Hirano et al. (US7022276).

Re claim 6, Kanzawa et al. show and disclose

The method for manufacturing a component built-in module according to claim 1,

Kanzawa et al. does not disclose

wherein the first electrical insulating sheet and the second electrical insulating sheet comprise 70 to 95 weight% of inorganic filler and 5 to 30 weight% of uncured thermosetting resin composition.

In the same field of an electronic device, Hirano et al. teaches:

wherein the first electrical insulating sheet and the second electrical insulating sheet comprise 70 to 95 weight% of inorganic filler and 5 to 30 weight% of uncured thermosetting resin composition. (a thermal conductive resin composition including 70 to 95 mass % of an inorganic filler and 5 to 30 mass % of a resin composition [ABSTRACT])

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the insulating layer of Kanzawa et al. by adapting same amount of inorganic filler and uncured thermosetting resin composition as taught by Hirano et al., in order to improve productivity and reduce the cost in processing the holes. (Hirano et al., [ABSTRACT]).

Art Unit: 2859

10. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kanzawa et al. in view of Kwong as applied to claim 1 above, and further in view of Sugaya et al. (US6931725).

Re claim 9, Kanzawa et al. show and disclose

The method for manufacturing a component built-in module according to claim 1,

Kanzawa et al. does not disclose

wherein after attaching a protective film to a principal surface of the third electrical insulating sheet, the via hole is formed so as to penetrate through the protective film and the third electrical insulating sheet.

In the same field of an electronic device, Sugaya et al. teaches:

wherein after attaching a protective film (a protective film [col. 4, line 45]) to a principal surface (bottom) of the third electrical insulating sheet, the via hole is formed (fig. 4) so as to penetrate through the protective film and the third electrical insulating sheet.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the electronic device of Kanzawa et al. by adding a protective film as taught by Sugaya et al., "thus the connection between the circuit component and the wiring pattern is stable and the reliability is further improved. " (Sugaya et al., [col. 4, line 49]).

Allowable Subject Matter

Art Unit: 2859

11. **Claims 10-13, 15-20 and 22-23 are objected** to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Claims 10, 17 and all claims dependent thereof are allowable over the art of record because the prior art does not teach or suggest that a module or an apparatus having,

For claim 10;

wherein the via hole is filled with the conductive resin paste by the steps of: (i) disposing the conductive resin paste on a principal surface of the third electrical insulating sheet; (ii) applying the conductive resin paste over the principal surface so that a paste layer made of the conductive resin paste with a predetermined thickness is formed around an opening of the via hole on the principal surface, while filling the via hole with the conductive resin paste; and (iii) scraping the paste layer off from the principal surface, while filling the via hole with the conductive resin paste.

For claim 17;

wherein after attaching a protective film to a principal surface of the third electrical insulating sheet, the via hole is formed so as to penetrate through the protective film and the third electrical insulating sheet; and

the via hole is filled with the conductive resin paste by the steps of: (i) disposing the conductive resin paste on a principal surface of the protective film; (ii) applying the

conductive resin paste over the principal surface of the protective film so that a paste layer made of the conductive resin paste with a predetermined thickness is formed around an opening of the via hole on the principal surface of the protective film, while filling the via hole with the conductive resin paste; and (iii) scraping the paste layer off from the principal surface of the protective film, while filling the via hole with the conductive resin paste.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to XIAOLIANG CHEN whose telephone number is (571)272-9079. The examiner can normally be reached on 7:00-5:00 (EST), Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-2800, ext 31. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Dean A. Reichard/
Supervisory Patent Examiner, Art Unit 2841

Xiaoliang Chen
Examiner
Art Unit 2841